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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,394	01/30/2004	Mami Kawabata	81790.0310	3798

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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

8/11

Office Action Summary	Application No.	Applicant(s)	
	10/768,394	KAWABATA ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-20* is/are allowed.

6)☒ Claim(s) *1-3 and 11* is/are rejected.

7)☒ Claim(s) *4-10, and 12-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01302004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

Figures 5-6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. Pages 3 (lines 1-2), 7 (lines 26-27), and 8 (lines 1-2) all relate these figures to "conventional" devices. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The title of the invention is not descriptive because "Semiconductor device" is generic. A new title is required that is clearly indicative of the invention to which the claims are directed. For example, --Selective switching of a transistor's back gate potential-- is more meaningful.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 11 recites the limitation "the N channel transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim. Was claim 11 meant to depend on claim 10?

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Manstretta et al. (Manstretta), in view of the applicants' conventional Figs. 5-6. Manstretta shows and discloses potential generator circuit 12 in Figs. 4-5 for generating first prescribed potential BODY, which is applied to a region of P channel transistors P1 and P2 (shown in Fig. 4). Fig. 5 shows potential generator circuit 12 with a first power supply terminal supplied with first power supply potential LV, a second power supply terminal supplied with second power supply potential HVloc that is higher than potential LV in at least the program mode (e.g. see column 4, lines 5-20), and an output terminal (i.e. the common node between P3 and P4) for outputting first

prescribed potential BODY. This configuration provides the highest of the power supply potentials as first prescribed potential BODY. For example, see column 3, lines 19-21, and 58-61. As shown in the tables of column 4, first power supply potential LV is set (e.g. at 5.5 V or at 3 V). Therefore, the level of LV is considered the predetermined potential, wherein if second power supply potential HVloc is higher than the predetermined potential, the higher HVloc will be output as first prescribed potential BODY, and if second power supply potential HVloc is lower than the predetermined potential, the higher LV will be output as first prescribed potential BODY. Although the reference does not clearly show or disclose transistors P1 and P2 with the first/second regions as recited within claim 1, one of ordinary skill in the art understands the use of regions (e.g. wells and substrate) with respect to MOS type transistors. Fig. 5 of the applicants' disclosure shows a conventional P-channel transistor receiving body potential Vpp/VB, and Fig. 6 shows a cross-sectional view of the transistor. Therefore, it would have been obvious to one of ordinary skill in the art to use the known P-channel transistor 40 of the applicants' figures, as the P-channel transistors P1 and P2 of Manstretta. Deeming one transistor a first transistor, it has second conduction type (P) second semiconductor region 52 (or 53) formed in first conduction type (N) first conduction region 51. First region 51 is supplied with first prescribed potential Vpp/VB (corresponding to Manstretta's BODY), and second region 52 (53) is supplied with second prescribed potential Vcc (VD). Therefore, claims 1 and 2 are rendered obvious. Since the predetermined potential (e.g. the set LV) is the same as first power supply potential LV, claim 3 is also rendered obvious.

Allowable Subject Matter

Claims 15-20 are allowed. There is presently no motivation to modify or combine any prior art reference(s) to ensure the potential generator circuit comprises the third transistor, as well as: 1) the inverter circuit as recited within claim 15 (upon which claim 16 depends), or 2) the comparator as recited within claim 17 (upon which claims 18-20 depend).

Also, claims 4-10, and 12-14 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no motivation to modify or combine any prior art reference(s) to ensure the potential generator circuit comprises the third transistor: and 1) the inverter circuit as recited within claim 4 (upon which claims 5-8 depend), or 2) the comparator as recited within claim 9 (upon which claims 10-14 depend).

Claim 11 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. Claim 11 depends on claim 9, which is only objected to as described above.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least sections of the claimed invention. The references of Jinbo, Teraoka et al., and Toyoyama et al. each shows and discloses circuitry that selectively switches the potential applied to the back gate of a MOS transistor. However, in each reference, the selected potential is determined by a mode signal, an input signal, or some other means. For example, see Jinbo (Fig. 8: VPP; VCC; transistors MP2,MP4; generator circuit 80; and signals G1-G4); Teraoka et al.

(Fig. 1: VP1; VP2; transistors P1,P2; generator circuit 3; and signal SELp); and Toyoyama et al. (Fig. 3: Vin; Vstbp; transistor 31; generator circuit 35; and signal Selectp).

The prior art references cited on the IDS submitted Jan 30, 2004 were reviewed and considered. The Japanese reference, and the Kobayashi reference, do not clearly show a transistor having its first prescribed potential (e.g. back gate bias) being selectable. The first prescribed potential of Watanabe's transistor 21 is the input voltage "in." Therefore, none of these references show or disclose the potential generator circuit for outputting the first prescribed potential as recited within each of the independent claims.

It is understood the present invention's voltage selection, for the first prescribed potential, is based on whether a second power supply potential is either higher or lower than a predetermined potential.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE
Terry L. Englund

11 February 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
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